

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Description

The M66591 is a general-purpose USB (Universal Serial Bus) device controller compliant with the Universal Serial Bus Specification Revision 2.0 and supports both Hi-Speed and Full-Speed transfer.

The USB Hi-Speed and Full-Speed transceiver are built-in, and the M66591 meets control, bulk and interrupt transfer types which are defined in the Universal Serial Bus Specification Revision 2.0.

The M66591 has 3.5K bytes FIFO and 7 endpoints (maximum) for data transfer.

Further, being equipped with the split bus (DMA interface) which is independent from the CPU bus interface, the M66591 is suitable for use of systems that require large capacity data transfer at Hi-Speed.

Features

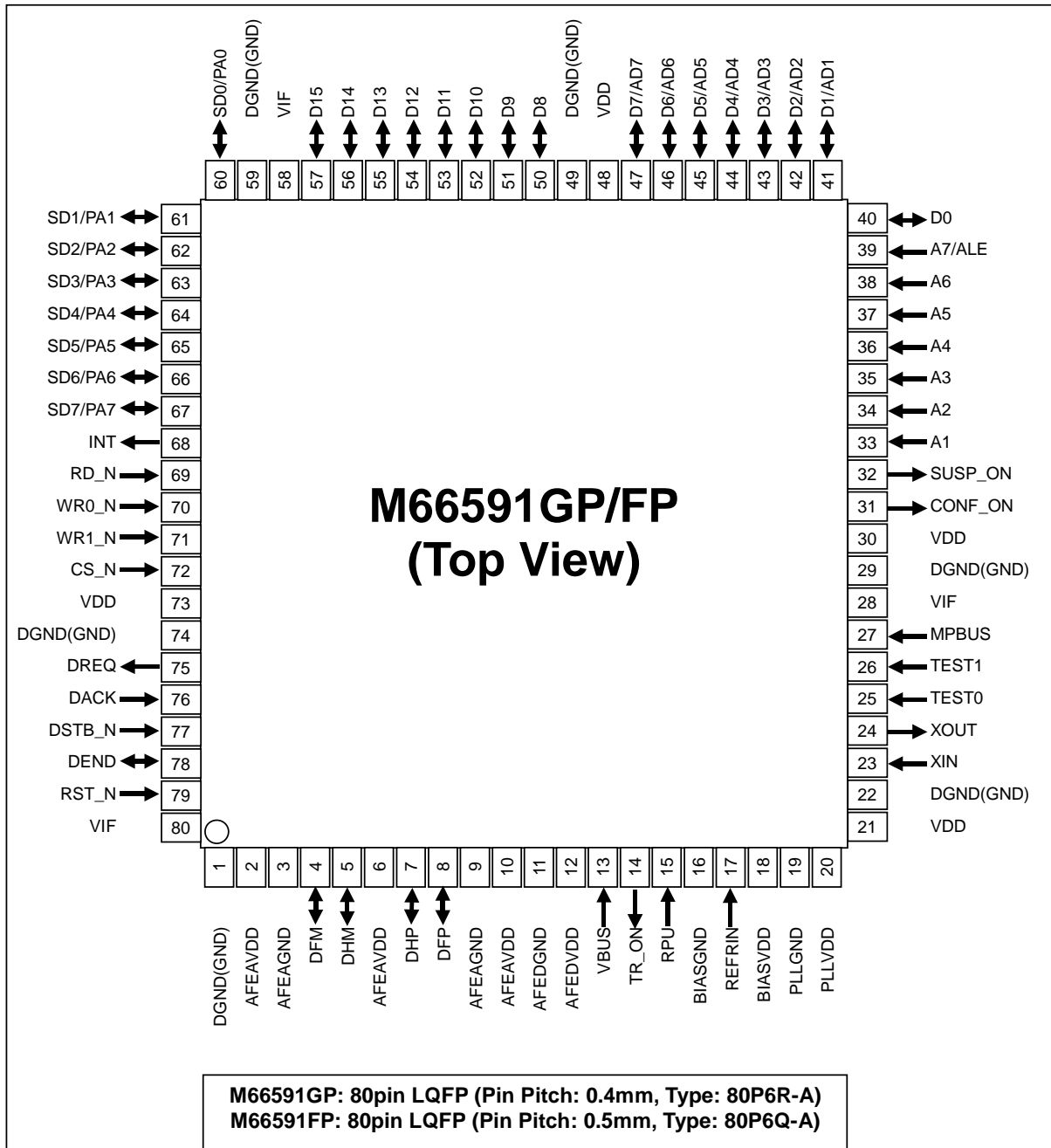
- Universal Serial Bus Specification Revision 2.0 compliant
- Built-in USB transceiver
- Supports both Hi-Speed (480M bps) and Full-Speed (12M bps)
- USB protocol layer by hardware
 - Bit stuffing encoding and decoding
 - CRC (Cyclic Redundancy Check) generation and checking
 - NRZI (Non Return Zero Invert) encoding and decoding
 - Packet detection
 - USB address checking
- Hi-Speed and Full-Speed detection by hardware
- Supports the following USB transfer types
 - Control transfer (EP0)
 - Bulk transfer (EP1~EP4)
 - Interrupt transfer (EP5~EP6)
- Built-in FIFO buffer (3.5K bytes) for endpoints
- Up to 7 endpoints selectable
- Data transfer condition selectable for each endpoint
 - Hi-Speed
 - EP0: Control transfer, continuous transfer mode, 256-byte FIFO
 - EP1~2: Bulk transfer, 512-byte FIFO, double buffer
 - EP3~4: Bulk transfer, 512-byte FIFO
 - EP5~6: Interrupt IN transfer, 64-byte FIFO
 - Full-Speed
 - EP0: Control transfer, continuous transfer mode, 256-byte FIFO
 - EP1~2: Bulk transfer, continuous transfer mode, 512-byte FIFO, double buffer
 - EP3~4: Bulk transfer, 512-byte FIFO
 - EP5~6: Interrupt IN transfer, 64-byte FIFO
- Automatic response for Set Address request
- Supports the following input frequency
 - 12 / 24 / 48MHz
- Supports 16-bit CPU I/F and 8/16-bit DMA transfer
- Supports separate/multiplex bus
 - 16-bit separate/multiplex bus
- Supports 8-bit split bus (DMA interface)
- USB status output for power management
- 1.8V/3.3V interface power supply

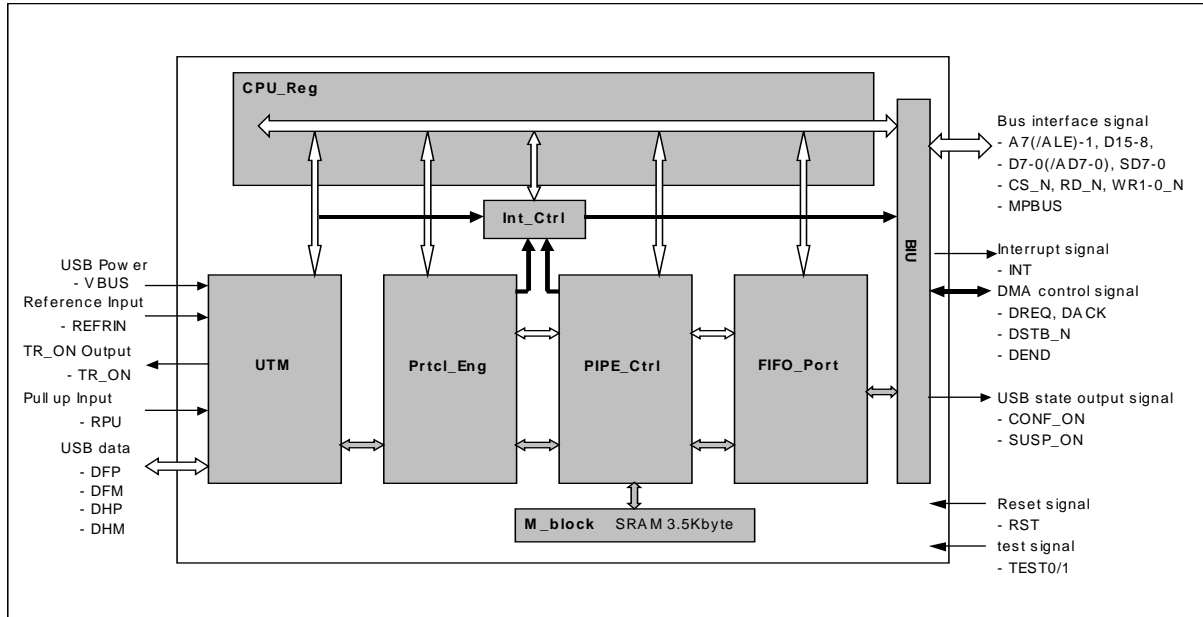
Application

Digital camera, printer, external storage device

Others, all PC peripheral using Hi-Speed USB

The Pin Layout





Block Description

The M66591 contains an USB transceiver block (UTM), a protocol engine block (Prtcl_Eng), a PIPE controller block (PIPE_Ctrl), a FIFO port block (FIFO_Port), an interrupt control block (Int_Ctrl) and a bus interface unit block (BIU).

- USB Transceiver (UTM)

The USB transceiver contains of a differential driver and a differential receiver. This USB transceiver compliant with the Universal Serial Bus Specification Revision 2.0 supports both Hi-Speed and Full-Speed transfer modes. Further, being equipped with an oscillation circuit/PLL (OSC PLL), the M66591 enables to supply 480MHz/48MHz clock signal by receiving external clock of 12, 24 or 48 MHz to be input.

- Protocol engine (Prtcl_Eng)

The protocol engine block controls data transfer such as bulk transfer and interrupt transfer by transaction control and transfer control. Also, this block is composed of a control transfer sequencer, an USB address register, an 8-byte USB request receiving register, and an automatic response circuit.

- Pipe controller (PIPE_Ctrl)

The PIPE controller block controls buffer states of transmit/receive data of each PIPE.

- FIFO Port (FIFO_Port)

The FIFO port block contains of two sets of FIFO ports. They are respectively referred to as C_FIFO port and D0_FIFO port, each being composed of 64 bits x 2 buffer registers, a sequencer, and a buffer write/read control circuit. Each FIFO port is connected to BIU with a 16-bit data line, enabling 8/16 setting by a program.

- Interrupt control (Int_Ctrl)

The interrupt control block transmits status signal that is transmitted from the protocol engine block and the PIPE controller block to the INT interrupt pin using the INT Pin Configuration Registers. Polarity of the interrupt pin can be set by a register.

- CPU Register (CPU_Reg)

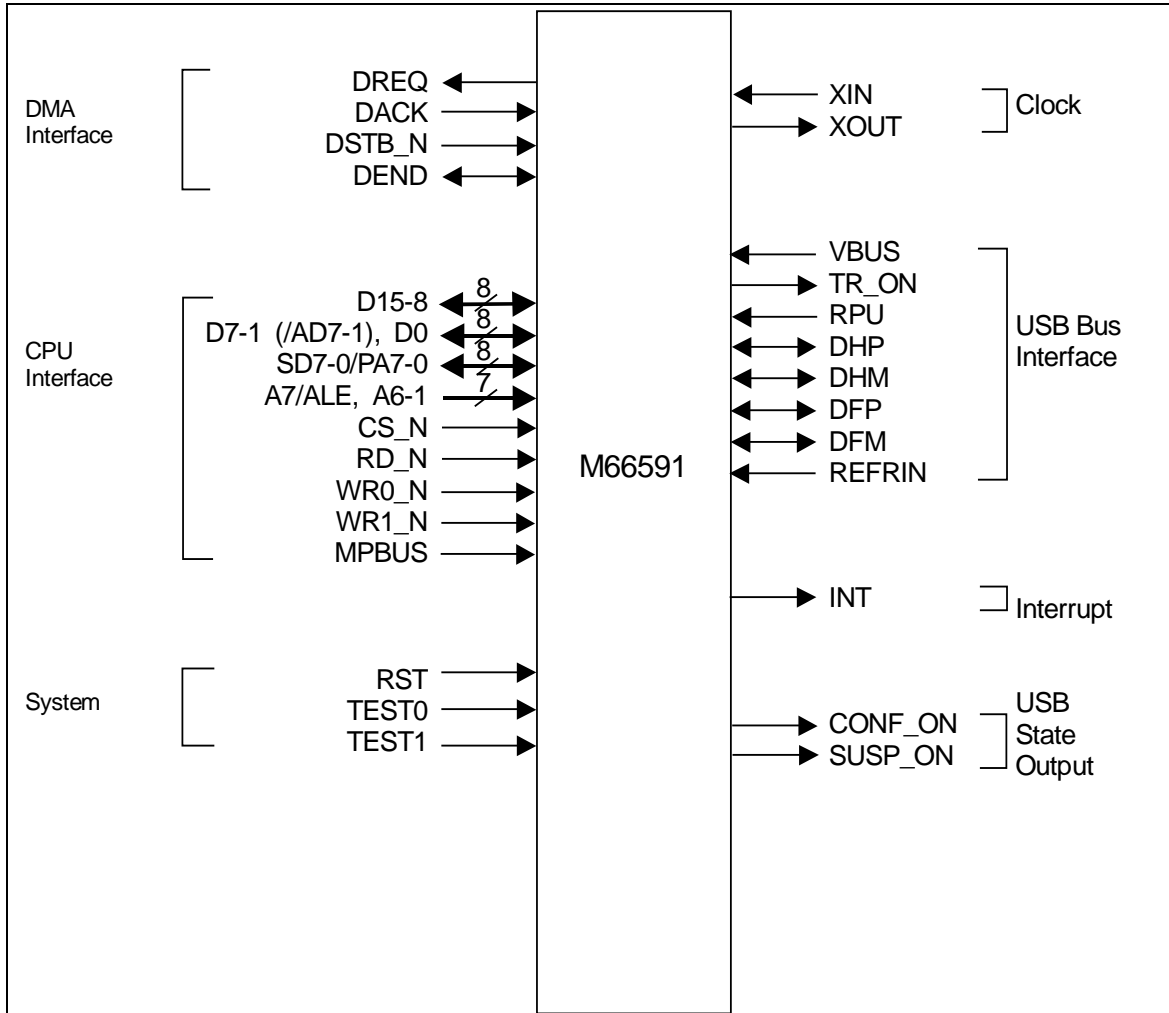
This is a CPU register block.

- Bus interface unit (BIU)

The bus interface unit block, in addition to the address decode and the data selector, has the following functions:

- (1) Separate bus/Multiplex bus select function
- (2) Data pin configuration function
- (3) Endian setting function of FIFO port
- (4) Data pin assignment function of D0_FIFO port
- (5) D0_FIFO port control pin configuration function
- (6) RD/WR with split bus (DMA Interface)
- (7) PIPE number assignment function of D0_FIFO port

Pin Functions



* The symbol “_N” of signal name means low active.

M66591GP/FP Pin Description

Item	Pin Name	Input/Output	Name / Function	Pin Count
CPU interface	D15-8	Input/Output	Data Bus These are data bus to access the register from the CPU.	8
	D7-1/AD7-1, D0	Input/Output	Data Bus / Address Bus When select to the 16-bit separate bus, these pins are used as D7-D0 of data bus. When select to the 16-bit multiplex bus, D7-D0 input/output and AD7-AD1 input are performed at time-sharing. In this case, D0 is not used.	8
	A7/ALE, A6-1	Input	Address Bus / Address Latch Enable When select to the 16-bit separate bus, these pins are address bus to access the register from the CPU. When select to the 16-bit multiplex bus, A7 becomes the ALE pin, latching addresses at the falling edge. A6 to A1 are not used.	7
	MPBUS	Input	Bus Mode Select The 16-bit separate bus is selected at low level. The 16-bit multiplex bus is selected at high level. This pin should not be switched after H/W reset.	1
	CS_N	Input	Chip Select When this pin is low level, the M66591 is selected.	1
	RD_N	Input	Read Strobe Data are read from registers at low level.	1
	WR1_N	Input	D15-8 Byte Write Strobe The data (D15-D8) are written to the register at the rising edge.	1
	WR0_N	Input	D7-0 Byte Write Strobe The data (D7-D0) are written to the register at the rising edge.	1
Interrupt interface	INT	Output	Interrupt Interrupts are requested to the CPU. Polarity of this pin can be set by a register.	1
DMA interface	SD7-0/PA7-0	Input/Output	Split Bus / General-purpose Port These pins are used to select whether the data bus of the split bus (DMA Interface) or the general-purpose port (GPIO). When the DB_Cfg bit is set to "0", the general-purpose port (GPIO) is selected. When the DB_Cfg bit is set to "1", the split bus is selected.	8
	DREQ	Output	DMA Request This pin is used to request DMA transfer of the D0_FIFO port. Polarity of this pin can be set by a register.	1
	DACK	Input	DMA Acknowledge DMA transfer of the D0_FIFO port is enabled in either low or high level. Polarity of this pin can be set by a register.	1
	DSTB_N	Input	Split Bus Strobe This pin is used as data strobe signal when the D0_FIFO port has set to the split bus (DMA Interface). When the RWstb bit of the Data Pin & FIFO/DMA Control Pin Configuration Register 2 is set to "1" (RD/WR strobe mode), this pin is used as data strobe signal.	1
	DEND	Input/Output	Transfer Complete When the PIPE direction is "IN", this pin receives transfer complete signal as an input signal from any other peripheral chip or the CPU. When the PIPE direction is "OUT", this pin indicates the last data transferred as the output signal. Polarity of this pin can be set by a register.	1
USB interface	DHP	Input/Output	USB Hi-Speed Data Connect the D+ signal of USB bus.	1

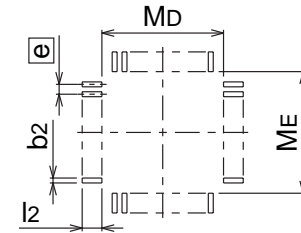
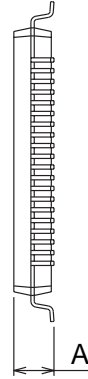
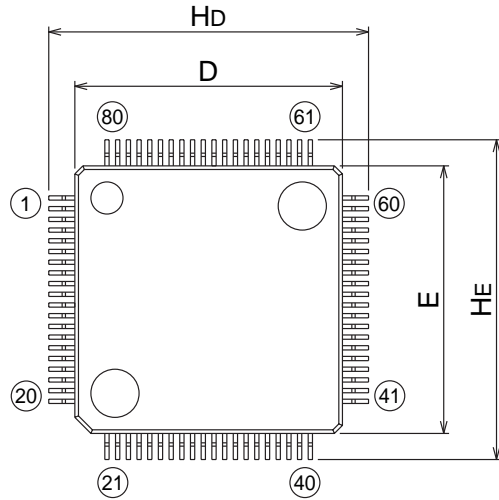
USB interface	DHM	Input/Output	USB Hi-Speed Data Connect the D- signal of USB bus.	1
	DFP	Input/Output	USB Full-Speed Data Connect this pin to DHP via a 43Ω±1% resistance.	1
	DFM	Input/Output	USB Full-Speed Data Connect this pin to DHM via a 43Ω±1% resistance.	1
	RPU	Input	Pull-up Control Connect this pin to TR_ON pin via a 1.5KΩ±5% resistance.	1
	TR_ON	Output	Pull-up Power Supply Output 3.3V power supply output for pull-up. This supply internally converts VBUS input from 5V to 3.3V and outputs it.	1
	VBUS	Input	VBUS Input Connect to the Vbus of USB bus. Connection or shutdown of the Vbus can be detected.	1
	REFRIN	Input	Reference Input Connect this pin to BIASGND via a 1.2KΩ±1% resistance.	1
USB status output	CONF_ON	Output	USB Configured Output This pin is used to indicate the transition to configured state which has performed after PC and USB enumeration.	1
	SUSP_ON	Output	USB Suspend Output This pin is used to indicate the transition to suspend state after the USB bus has detected idle state for 3ms.	1
Clock	XIN	Input	Oscillator Input These pins are used to input/output the signals of internal clock oscillation circuits. Connect a crystal unit between Xin and Xout pins. Oscillator Output If an external clock signal is used, input it to the Xin and Xout should be opened.	1
	XOUT	Output		1
System control	RST_N	Input	Reset This pin is used to initialize the values of the internal register or the counter at low level.	1
	TEST1-0	Input	Test These pins are input for the test. Fix to low level or keep open.	2
Power supply	AFEAVDD	Input	Analog Power Supply Connect to the 3.3V power supply.	3
	AFEAGND	Input	Analog Ground	2
	AFEDVDD	Input	USB Transceiver Digital Power Supply Connect to the 3.3V power supply.	1
	AFEDGND	Input	USB Transceiver Digital Power Ground	1
	BIASVDD	Input	BIAS Power Supply Connect to the 3.3V power supply.	1
	BIASGND	Input	BIASGND	1
	PLLVDD	Input	PLL Power Supply Connect to the 3.3V power supply.	1
	PLLGND	Input	PLLGND	1
	VDD	Input	Core Power Supply Connect to the 3.3V power supply.	4
	VIF	Input	IO Power Supply Connect to the 1.8V or 3.3V power supply.	3
	DGND	Input	Digital Ground	6

80P6R-A

MMP

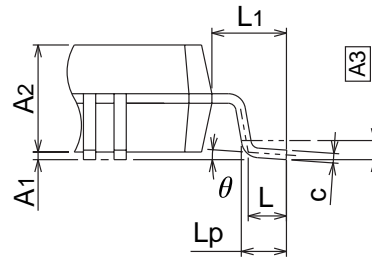
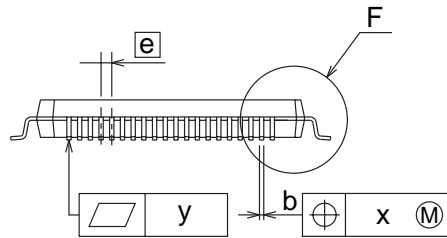
Plastic 80pin 10X10mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1010-0.4	-		Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.23
c	0.105	0.125	0.175
D	9.9	10.0	10.1
E	9.9	10.0	10.1
e	-	0.4	-
H _D	11.75	11.95	12.15
H _E	11.75	11.95	12.15
L	0.35	0.5	0.65
L ₁	-	0.975	-
L _p	0.45	0.6	0.75
A ₃	-	0.25	-
x	-	-	0.07
y	-	-	0.1
θ	0°	-	8°
b ₂	-	0.225	-
l ₂	1.0	-	-
MD	-	10.4	-
ME	-	10.4	-

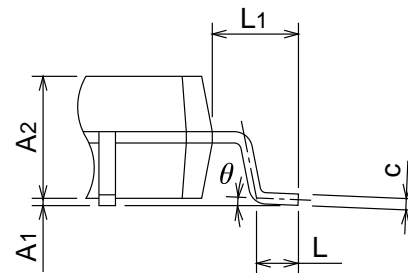
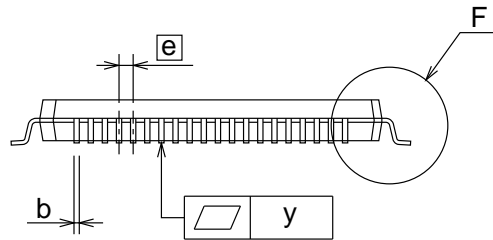
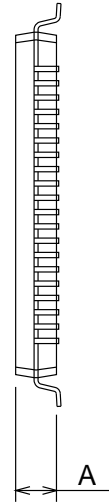
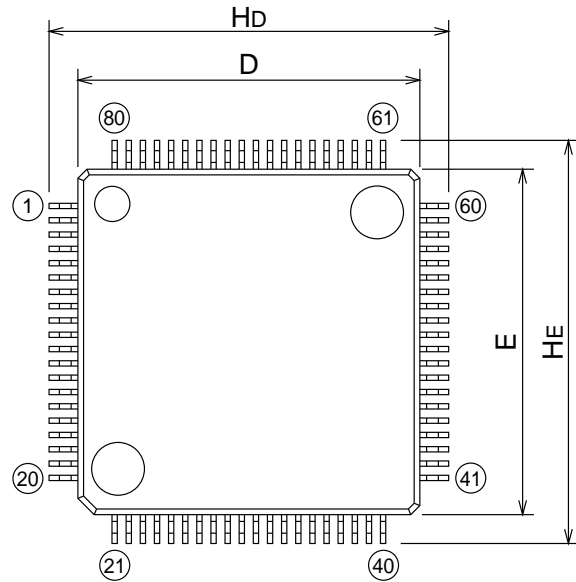


Detail F

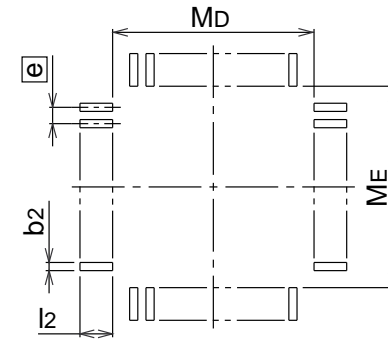
80P6Q-A

Plastic 80pin 12X12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	-		Cu Alloy



Detail F



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	-	0.5	-
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	-	1.0	-
y	-	-	0.1
θ	0°	-	10°
b2	-	0.225	-
l2	1.0	-	-
MD	-	12.4	-
ME	-	12.4	-